Fig. 5 is a circuit diagram of a pixel in the light emitting device to which the repairing method of the present invention is applied. Each pixel has a source signal line Si (i represents one of integers from 1 to x), a power supply line Vi (i represents one of integers from 1 to x), a writing gate signal line Gaj (j represents one of integers from 1 to y) and an erasing gate signal line Gej (j represents one of integers from 1 to y).

Each pixel also has a switching TFT 501a, an erasing TFT 501b, an EL driving TFT 502, an EL element 503, and a capacitor 504.

The switching TFT 501a has a gate electrode connected to the writing gate signal line Gaj. The switching TFT 501a has a source region and a drain region one of which is connected to the source signal line Si and the other of which is connected to a gate electrode of the EL driving TFT 502.

The erasing TFT 501b has a gate electrode connected to the erasing gate signal line Gej. The erasing TFT 501 has a source region and a drain region one of which is connected to the power supply line Vi and the other of which is connected to the gate electrode of the EL driving TFT 502.

The EL driving TFT 502 has a source region connected to the power supply line Vi, and has a drain region connected to one of two electrodes of the EL element 503. The other electrode of the two electrodes of the EL element 503, namely, the electrode that is not connected to the drain region of the EL driving TFT 502, is connected to an opposite power supply 507.

Of the two electrodes of the EL element 503, the one that is connected to the drain region of the EL driving TFT 502 is called a pixel electrode while the one that is connected to the opposite power supply 507 is called an opposite electrode.

The capacitor 504 is formed between the gate electrode of the EL driving TFT

502 and the power supply line Vi.

Fig. 6A shows a pixel portion of the light emitting device which has a plurality of pixels shown in Fig. 5. A pixel portion 506 has source signal lines S1 to Sx, power supply lines V1 to Vx, writing gate signal lines Ga1 to Gay, and erasing gate signal lines Ge1 to Gey. The plural pixels 505 form a matrix in the pixel portion 506.

Fig. 6B shows the operation of the TFTs and the level of voltage to be inputted to the power supply line Vi and to the opposite electrode in each pixel during repairing a defect portion of the EL element 503. When the defect portion of the EL element 503 is to be repaired, the switching TFT 501a and the EL driving TFT 502 in each pixel are both turned ON. The erasing TFT 501b in each pixel is turned OFF. While the voltage of the power supply line Vi is kept constant, the voltage of the opposite electrode is changed at given time intervals so that a given reverse bias current flows into the EL element 503 at given time intervals.

The defect portion of the EL element 503 may be repaired at once in all of the pixels 505 of the pixel portion 506. Alternatively, the repair may be performed on one line of pixels at a time, or on one pixel at a time.

The method of the present invention can increase the amount of current actually flowing through the EL layer upon application of a forward bias voltage to the EL element even if a pin hole is formed in the EL layer during formation of the layer due to dusts or the like and two layers sandwiching a light emitting layer short-circuit, because the method can raise the resistance of the defect portion where the short circuit takes place by changing the defect portion into the transmuted portion. Therefore the repairing method of the present invention can raise the luminance of emitted light with application of the same level of voltage despite the presence of the defect portion.

Having high resistance R_{SC}, the transmuted portion hardly allows a current to

flow therein in contrast to the defect portion where there is always a flow of current to accelerate degradation of a part of the EL layer that surrounds the defect portion. Therefore, degradation is not accelerated in a part of the EL layer that surrounds the transmuted portion.

[Embodiment 3]

In this embodiment, the structure of the driver circuit which is driving the pixel portion in Embodiment 1 is explained in Embodiment 1. The source signal driving circuit and the gate signal driving circuit which are driving the pixel portion in Embodiment 1 are not limited to the structure shown in this Embodiment.

Fig. 7 shows a driving circuit of the light emitting device by a block figure. In Fig. 7A, the reference numeral 601 is a source signal line driver circuit which has the shift register 602, the latch (A) 603 and the latch (B) 604.

A clock signal (CLK) and a start pulse (SP) are inputted to the shift register 602 in the source signal line driving circuit 601. The shift register 602 generates timing signals in order based upon the clock signal (CLK) and the start pulse (SP), and the timing signals are supplied one after another to downstream circuits through a buffer (not shown in the figure).

Note that the timing signals from the shift register 602 may be buffer-amplified by a circuit such as a buffer. The load capacitance (parasitic capacitance) of a wiring to which the timing signals are supplied is large because many of the circuits and elements are connected to the wiring. The buffer is formed in order to prevent dullness in the rise and fall of the timing signal, generated due to the large load capacitance. In addition, the buffer is not always necessary formed.

The timing signals which is a buffer-amplified are supplied to the latch (A) 603. The latch (A) 603 has a plurality of latch stages for processing an n-bit digital signal